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Identification of Double Quantum Dots in Nanowire Devices by Single-Gate Sweeps

Hiroshi Inokawa[1]* and Yasuo Takahashi[2]

[1]*Research Institute of Electronics, Shizuoka University, Hamamatsu 243-8011, Japan*
[2]*Graduate School of Information Science and Technology, Hokkaido University, Sapporo 060-0814, Japan*

E-mail: inokawa06@rie.shizuoka.ac.jp

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The drain current-gate voltage characteristics of the double quantum dot devices are classified theoretically based on periodic multiple peaks separated by deep valleys, and are observed experimentally in silicon nanowire devices. Inspired by the unique patterns in the characteristics, delta-literals for multiple-valued logic are proposed as a new application of the double quantum dots.

1. Introduction

Despite advances in microfabrication technology, it is still difficult to precisely control the dimensions of 10 nm or less. Therefore, randomness in sizes [1], [2], dopant positions [3], etc. is often utilized to naturally form quantum dots for single-electron devices and qubits of quantum computing [4]. Out of naturally formed devices, it is rather easy to select single-dot one due to the periodic Coulomb oscillation, but it is not straightforward to identify double dots or more. In this report, for efficient identification of double quantum dots, complex oscillation patterns in the single-gate drain current-gate voltage (I_d-V_{gs}) characteristics are classified based on simulation, and then real examples corresponding to the classification are found in silicon nanowire devices.

2. Theoretical Prediction

The charging states of the double quantum dots can be described by the honeycomb diagram [5], where numbers of electrons in the dots are fixed in each hexagonal domain, and current flows only at triple points.

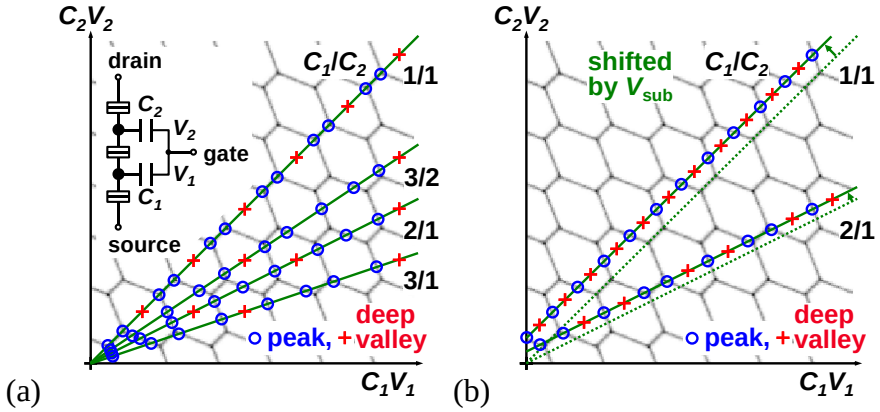

Fig. 1. (a) Honeycomb diagram [5] and trajectories of single-gate sweeps for different ratios of C_1 and C_2. (b) Trajectories shifted by the substrate voltage V_{sub}.

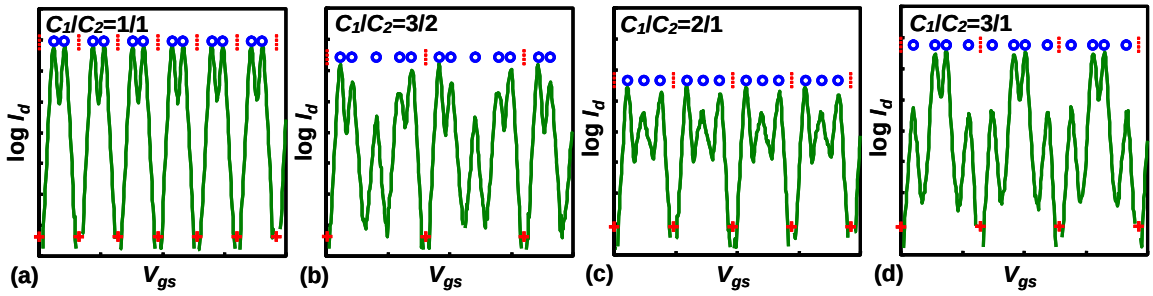

Fig. 2. Simulated I_d-V_{gs} characteristics of double quantum dot devices corresponding to Fig. 1(a) for different C_1/C_2 ratios of (a) 1/1, (b) 3/2, (c) 2/1 and (d) 3/1. Normalized temperature and drain voltage are about 0.06 and 0.08 (e.g. 20 K and 5 mV for junction capacitance of 1 aF and C_1+C_2=1 aF), respectively.

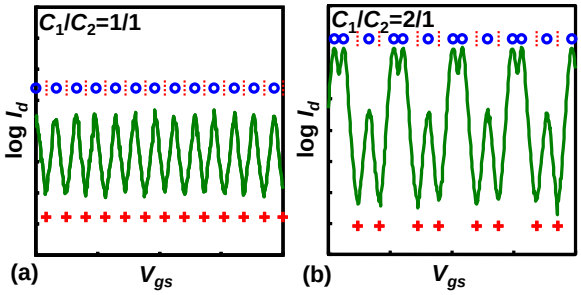

Fig. 3. Simulated I_d-V_{gs} characteristics shifted by the substrate voltage as shown in Fig. 1(b). C_1/C_2 ratios are (a) 1/1 and (b) 2/1, respectively.

However, at a finite temperature, current also flows at domain boundaries due to thermal excitation resulting in unique periodic oscillations in single-gate I_d-V_{gs} characteristics. As shown in Fig. 1(a), depending on the gate capacitance ratio C_1/C_2, trajectories of single-gate sweeps pass through different area of the diagram, causing current peaks (o) at the triple points and boundaries, and deep valleys (+) at the center of hexagons. The expected characteristics are simulated by the Monte Carlo simulator SIMON [6]. If C_1/C_2 are 1/1, 3/2, 2/1 and 3/1, I_d-V_{gs} characteristics with 2, 5, 3 and 4 peaks separated by deep valleys are obtained as can be seen in Fig. 2 (a), (b), (c) and (d), respectively. We can also make a parallel shift of the trajectory and electrically adjust the I_d-V_{gs} characteristics by changing the substrate voltage V_{sub} if the gate and substrate have different capacitance ratios to the dots, that is $C_1/C_2 \neq C_3/C_4$, where C_3 and C_4 are capacitances between substrate and quantum dots on the source and drain sides, respectively. Figure 1(b) shows the shift of the trajectories by the substrate voltage in the cases of C_1/C_2=1/1 and 2/1, and Figs. 3 (a) and (b) show the corresponding I_d-V_{gs} characteristics. Periodic characteristics may appear for C_1/C_2=1/1 [Fig.3 (a)], and single and double peaks separated by deep valleys may appear alternately for C_1/C_2=2/1 [Fig.3 (b)], depending on the substrate voltage.

3. Experiments

Silicon nanowire devices are fabricated by delineating undoped silicon-on-insulator (SOI) by electron beam lithography. The original width W, length L and thickness of the nanowires are 44~50, 50~70 and 30 nm, respectively, and further reduced by thermal oxidation corresponding to SiO_2 thickness of 50 nm on (100) surface. The buried oxide thickness is 400 nm.

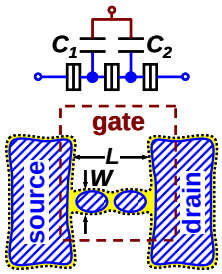

Fig. 4. Schematic structure of the silicon nanowire device with double quantum dots.

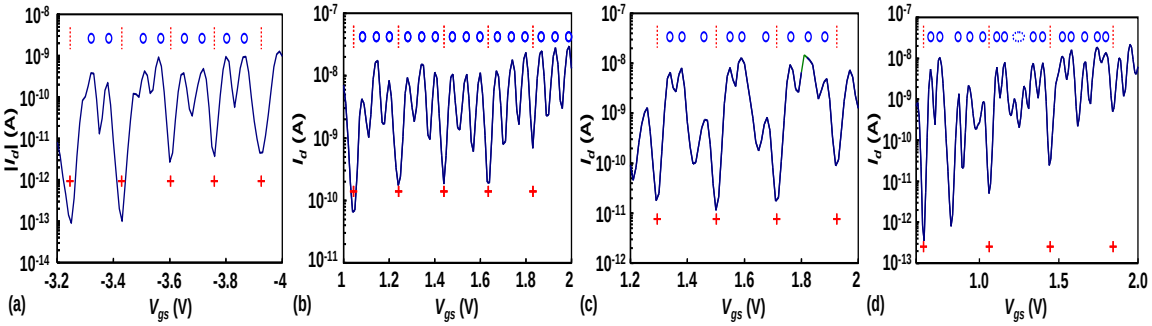

Fig. 5. I_d-V_{gs} characteristics of the silicon nanowire devices measured at T=25 K and $|V_{ds}|$=10 mV. Estimated C_1/C_2 ratios are (a)~1/1, (b)~2/1, (c)~2/1 and (d)~3/2, respectively.

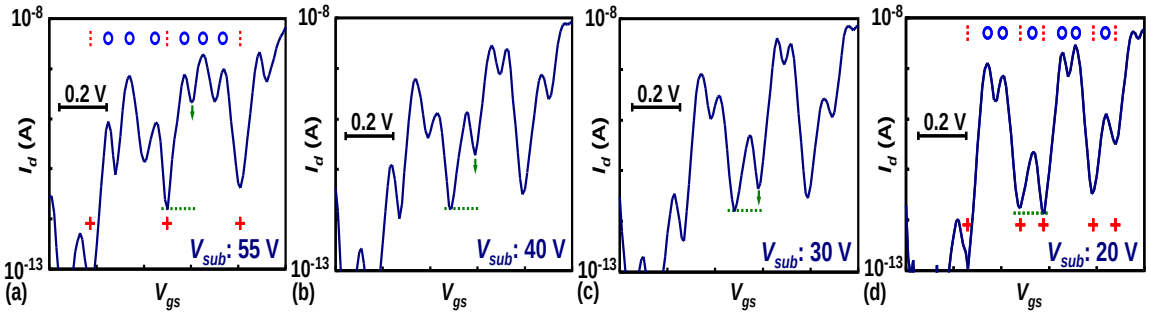

Fig. 6. I_d-V_{gs} characteristics for different substrate voltages V_{sub} measured at T=25 K and V_{ds}=10 mV. Estimated C_1/C_2 ratios is ~2/1. (a) corresponding to Fig. 2(c) evolves into (d) corresponding to Fig. 3(b). V_{gs} is shifted so that the peak position is fixed.

Size fluctuations together with quantum confinement effect [2], [7] and oxidation-induced strain [7] naturally form double quantum dots as schematically shown in Fig. 4. C_1/C_2 ratio also varies due to the fluctuation in the quantum dot sizes and the gate alignment. As shown in Fig. 5, we could successfully observe the unique I_d-V_{gs} characteristics with multiple peaks separated by deep valleys. Substrate voltage dependence in Fig. 6 also supports the presence of the double quantum dots, since the evolution of the characteristics in Fig. 2(c) into those in Fig. 3(b) can be clearly observed.

3. Application to Delta-Literals

It has been proposed that the periodic input-output characteristics of single quantum dot device, i.e. single-electron transistor, are suitable for multiple-valued logics (MVLs) in that the number of devices in circuits, power consumption, delay time, and wiring complexity can be largely reduced

[8]-[10].

Table I. Truth tables of (a) 3-valued and (b) 4-valued delta-literals.

(a)

input	output x^0	x^1	x^2
0	H	L	L
1	L	H	L
2	L	L	H

(b)

input	output x^0	x^1	x^2	x^3
0	H	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	L	L	H

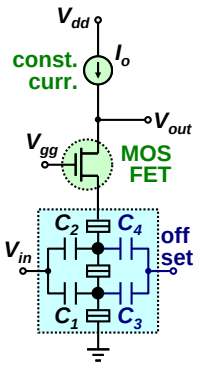

Fig. 7. Proposed 3- or 4-valued delta-literal with double quantum dot device having C_1/C_2=1/1 or 2/1.

Here we propose the use of double quantum dot devices with C_1/C_2=1/1 and 2/1 as components for 3- and 4-valued delta-literals [11], which are the basic circuits of MVLs and whose truth tables are shown in Tables I (a) and (b), respectively. By combining the double quantum dot devices with a MOSFET and a constant-current source I_o [8]-[10] as in Fig. 7, the deep valleys and peaks in I_d-V_{gs} characteristics can be assigned to H and L outputs, respectively, to realize the delta-literals. Note that the 3 or 4 kinds of literals, x^0, x^1, x^2 and x^3, can be obtained by shifting I_d-V_{gs} characteristics with different offset voltages. Since the conventional delta-literal requires 2~5 MOSFETs [12], the use of the double quantum dot device greatly simplify the MVL circuits.

3. Conclusion

Unique I_d-V_{gs} characteristics with multiple peaks separated by deep valley were theoretically assigned to double quantum dot structure, and examples were found in silicon nanowire devices. It was proposed that the double quantum dot devices with the capacitance ratio C_1/C_2=1/1 and 2/1 can be used for delta-literals for MVL, which can reduce the device count to a half compared to the conventional circuit.

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References

[1] K. Uchida, J. Koga, R. Ohba, and A. Toriumi, IEEE Trans. Electron Devices **50**, 1623 (2003).
[2] R. Suzuki, M. Nozue, T. Saraya, and T. Hiramoto, Jpn. J. Appl. Phys. **52**, 104001 (2013).

[3] Y. Ono, K. Nishiguchi, A. Fujiwara, H. Yamaguchi, H. Inokawa, and Y. Takahashi, Appl. Phys. Lett. **90**, 102106 (2007).
[4] H. W. Liu, T. Fujisawa, Y. Ono, H. Inokawa, A. Fujiwara, K. Takashina, and Y. Hirayama, Phys. Rev. B **77**, 073310 (2008).
[5] H. Grabert and M. H. Devoret, *Single Charge Tunneling* (Plenum Press, New York, 1992) Chap. 3, p. 109.
[6] C. Wasshuber, H. Kosina, and S. Selberherr, IEEE Trans. Comput. Aided Design **16**, 937 (1997).
[7] S. Horiguchi, M. Nagase, K. Shiraishi, H. Kageshima, Y. Takahashi, and K. Murase, Jpn. J. Appl. Phys. **40**, L29 (2001).
[8] H. Inokawa, A. Fujiwara, Y. Takahashi, Appl. Phys. Lett. **79**, 3618 (2001).
[9] H. Inokawa, A. Fujiwara, Y. Takahashi, Jpn. J. Appl. Phys. **41**, 2566 (2002).
[10] H. Inokawa, A. Fujiwara, Y. Takahashi, IEEE Trans. Electron Devices **50**, 462 (2003).
[11] K. Degawa, T. Aoki, T. Higuchi, H. Inokawa, and Y. Takahashi, IEICE Trans. Electron. **E87C**, 1827 (2004).
[12] Y. Yasuda, Y. Tokuda, S. Zaima, K. Pak, T. Nakamura, and A. Yoshida, IEEE J. Solid-State Circuits **SC-21**, 162 (1986).